IN THE CLAIMS

1. (Previously Amended) A data processing system comprising:

a. a system bus;

b. a processor with a system controller containing a semi-store-in level one cache memory having an associated duplicate tag memory responsively coupled to a dedicated level two cache memory having an associated tag memory which is responsively coupled via said system bus to a level three cache memory which is directly coupled to at least one memory storage unit;

c. a circuit for directly SNOOPing said system bus; and

d. First logic which invalidates a corresponding level one cache memory location in response to a non-local memory write request generated by another processor.

2. (Previously Presented) A data processing system according to claim 1 further comprising second logic which inhibits said first logic from invalidating said corresponding level one cache memory location in response to said non-local memory write request generated by another processor for mode 3 requests without ownership.

3. (Previously Presented) A data processing system according to claim 1 further comprising:

a. Third logic which invalidates said corresponding level one cache memory location in response to a SNOOP hit.

4. (Previously Presented) A data processing system according to claim 3 further comprising:

a. Fourth logic which records location of data within the level one cache memory in response to a level one cache memory read miss and a level two cache memory read miss.

5. (Previously Presented) A data processing system according to claim 4 further comprising:

a. Fifth logic which detects a parity error in said level two cache memory and which in response invalidates said corresponding level one cache memory location to avoid loss of control between said level one cache memory and said level two cache memory.

6. (Previously Presented) A data processing system comprising:

a. A processor having a level one cache memory within a system controller;

b. A level two cache memory located within said system controller dedicated to said processor and responsively coupled to said level one cache memory;

c. a system bus;

d. A memory storage unit;

e. A level three cache memory responsively coupled to said level two cache memory via said system bus and responsively coupled to said memory storage unit; and

f. A first circuit which invalidates a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory hit.

7. (Previously Presented) A data processing system according to claim 6 further comprising:

a. A second circuit which inhibits said first circuit from said invalidating in response to a mode 3 request with lack of ownership.

8. (Previously Presented) A data processing system according to claim 7 further comprising:

a. A third circuit which SNOOPs said system memory bus; and

b. A fourth circuit which invalidates said corresponding portion of said level one cache memory in response to a SNOOP hit from a write request by another processor.

9. (Previously Presented) A data processing system according to claim 8 further comprising:

a. A fifth circuit which records in said level one cache memory location of data in response to a level one cache memory read miss and a level two cache memory read miss.

10. (Previously Presented) A data processing system according to claim 9 further comprising:

a. A sixth circuit which detects parity errors of said level two cache memory and invalidates said corresponding portion which is less than all of said level one cache memory in response to said detected parity error.

11. (Previously Presented) A method of maintaining validity of data within a semi-store-in level one cache memory of a processor located within a system controller containing a duplicate tag memory and responsively coupled to a level two cache memory which is dedicated to said processor, which is located within said system controller having a tag memory, and which is responsively coupled to a system memory bus comprising:

a. Formulating a write memory request within said processor;

b. First checking for a level one cache memory hit in response to said write memory request;

c. Second checking for a level two cache memory hit in response to a hit found by said first checking step; and

d. Invalidating a portion of said level one cache memory corresponding to said write memory request in response to a hit found by said second checking step as indicated by said duplicate tag memory.

12. (Previously Presented) A method according to claim 11 further comprising:

a. Inhibiting said invalidating step if said write memory request is mode 3 lacking ownership identification by said duplicate tag memory.

13. (Previously Presented) A method according to claim 12 further comprising:

a. SNOOPing said system memory bus; and

b. Invalidating said portion of said level one cache memory if said SNOOPing step identifies data corresponding to said write memory request.

14. (Previously Presented) A method according to claim 13 further comprising:

a. Formulating a read memory request;

b. experiencing a level one cache memory read miss; and

c. recording location of data corresponding to said read memory request in said level one cache memory.

15. (Previously Presented) A method according to claim 14 further comprising:

a. Determining whether a reference to said level two cache memory has caused a parity error; and

b. Invalidate said portion which is less than all of said level one cache memory in response to said determining said parity error.

16. (Previously Presented) An apparatus comprising:

a. executing means for executing program instructions;

b. level one semi-store-in caching means located within a system controller and responsively coupled to said executing means for level one caching data;

c. accessing means responsively coupled to said executing means and said level one semi-store-in caching means for accessing a data element from said level one semi-store-in means if said executing means requires accessing of said data element;

d. level two caching means located within said system controller and responsively coupled to said requesting means for level two caching data and dedicated to said executing means; and

e. first invalidating means responsively coupled to said level one semi-store-in caching means for invalidating said data element within said semi-store-in caching means if said data element is a write data element located within said level two caching means and within said semi-store-in level one caching means.

17. (Previously Presented) An apparatus according to claim 16 further comprising:

a. inhibiting means responsively coupled to said first invalidating means for inhibiting said invalidating if said data element is mode 3 without ownership within said semi-store-in caching means.

18. (Previously Presented) An apparatus according to claim 17 further comprising:

a. bussing means responsively coupled to said level two caching means for bussing system memory data;

b. SNOOPing means responsively coupled to said bussing means for SNOOPing said bussing means; and

c. second invalidating means responsively coupled to said SNOOPing means for invalidating said data element if said SNOOPing means locates a corresponding data element and said data element is a write data element.

19. (Previously Presented) An apparatus according to claim 18 further comprising:

a. retrieving means responsively coupled to said level two caching means for retrieving a location of said data element if said data element is a read data element and said level two caching means experiences a miss.

20. (Previously Presented) An apparatus according to claim 19 further comprising:

a. detecting means responsively coupled to said level two caching means for detecting a parity error; and

b. third invaliding means responsively coupled to said level one semi-store-in caching means and said detecting means for invalidating said data element within said level one semi-

store-in caching means if said detecting means detects said parity error.

21. (Canceled) An apparatus comprising:

a. an instruction processor;

b. a level one cache memory directly coupled to said instruction processor;

c. a level two cache memory directly coupled to said level one cache memory;

d. a data element having a parity error stored in said level two cache memory; and

f. a facility responsively coupled to said level one cache memory and said level two cache memory which detects said parity error of said data element and invalidates a corresponding data element within said level one cache memory.

22. (Canceled) An apparatus according to claim 21 wherein said level one cache memory further comprises a level one instruction cache memory and a level one operand cache memory.

23. (Canceled) An apparatus according to claim 22 further comprising an invalidation circuit which invalidates a write data element within said level one cache memory if said instruction processor initiates a write request to said write data element

resulting in a hit within said level one cache memory and also a hit on a corresponding write data element within said level two cache memory.

24. (Canceled) An apparatus according to claim 23 further comprising a SNOOPing circuit.

25. (Canceled) An apparatus according to claim 24 wherein said write data element is located within said level one operand cache memory.